

CLAIMS

What is claimed is:

1. A memory controller comprising:

5 a first port and a second port which receive and transmit an N-bit data value, respectively;

a third port receiving and transmitting a 2N-bit data value; and

a fourth port and a fifth port, each receiving and transmitting an N-bit data value;

10 wherein during a first operation, two N-bit data values are simultaneously fetched from a memory device corresponding to the first port via the first port and from a memory device corresponding to the second port in response to a command signal and an address input received via the third port, the two fetched N-bit data values are combined into a 2N-bit data value, and the 2N-bit data value is transmitted to the third port, and

15 wherein during a second operation, the N-bit data value is fetched from at least one of the corresponding memory devices via the at least one corresponding first port and second port in response to a command signal and address input via at least one of the fourth port and fifth port, and the fetched N-bit data value is transmitted to the at least one of the fourth port and fifth port.

20 2. The memory controller of claim 1, wherein the 2N-bit data value input via the third port is divided into two N-bit data values and the two N-bit data values are output to the corresponding memory devices via the first and second ports, respectively.

25 3. The memory controller of claim 1, wherein the N-bit data value input via the at least one of the third port and the fourth port is output to the corresponding memory device via the at least one of the first port and the second port.

30 4. The memory controller of claim 1, wherein the command signal comprises a signal for fetching data.

5. The memory controller of claim 1, wherein the first and second ports are connected to the corresponding memory devices via independent N-bit buses.

6. The memory controller of claim 1, wherein the third port is connected to a 2N-bit device via a 2N-bit bus, and receives and transmits the 2N-bit data values.

7. The memory controller of claim 1, wherein the third port is connected to a 2N-bit central processing unit (CPU) via a 2N-bit bus and receives and transmits the 2N-bit data values.

8. The memory controller of claim 1, wherein the fourth and fifth ports are connected to a corresponding N-bit device via independent N-bit buses.

9. The memory controller of claim 1, wherein N is 32.

10. A computer system comprising:  
 at least two memory devices which store data and instructions;  
 at least one 2N-bit device which controls and manages the computer system;  
 at least two N-bit devices exchanging data with the memory devices; and  
 a memory controller which controls the exchange of data among the memory devices and the 2N-bit device, and among the memory devices and the at least two N-bit devices;  
 wherein the memory controller comprises:  
 a first port and a second port which receive and transmit N-bit data values from and to the corresponding memory devices via corresponding N-bit buses;  
 a third port which receives and transmits 2N-bit data values from and to the 2N-bit device via a 2N-bit bus; and  
 a fourth port and a fifth port, each receiving and transmitting an N-bit data value from and to a corresponding N-bit device via a corresponding N-bit bus, and  
 wherein, in response to a command signal and address that are generated by the 2N-bit device and input via the third port, the memory controller simultaneously fetches

the N-bit data values from the memory devices corresponding to the address via the first and second ports, combines the N-bit data values to form a fetched 2N-bit data value, and transmits the fetched 2N-bit data value via the third port, and

wherein, in response to a command signal and address that are generated by the corresponding N-bit device and input via at least one of the fourth port and the fifth port, the memory controller fetches the N-bit data value from a memory device corresponding to the address via at least one of the first port and the second port and transmits the fetched N-bit data value via at least one of the fourth port and the fifth port.

11. The computer system of claim 10, wherein the memory controller divides the 2N-bit data value into N-bit data values and outputs the divided N-bit data values to the corresponding memory devices via the corresponding first port and second port, the 2N-bit data value being generated by the 2N-bit device and input via the third port.

12. The computer system of claim 10, wherein the memory controller outputs the N-bit data value to the memory device via at least one of the first port and second port, the N-bit data value being generated by the corresponding N-bit device and input via at least one of the third port and the fourth port.

13. The computer system of claim 10, wherein the command signal comprises a signal for fetching data.

14. A data transmission method performed by a memory controller including first and second ports receiving and transmitting N-bit data values, a third port which receives and transmits 2N-bit data values, and fourth and fifth ports which receive and transmit N-bit data values, the method comprising:

receiving at least one of a command signal and address input via the third port, and a command signal and address input via at least one of the fourth and fifth ports; and

simultaneously fetching N-bit data values from corresponding memory devices via the first and second ports in response to the command signal and address input via

the third port, combining them to form a fetched 2N-bit data value and transmitting the fetched 2N-bit data value, and

fetching the N-bit data value from at least one of the corresponding memory devices via at least one of the first port and the second port in response to the command signal and address input via the at least one of the fourth port and the fifth port, and transmitting the fetched N-bit data value to the at least one of the fourth port and the fifth port.

15. The method of claim 14, wherein the 2N-bit data value input via the third port is divided into two N-bit data values and the divided two N-bit data values are output to the corresponding memory devices via the first and second ports.

16. The method of claim 14, wherein the N-bit data value input via the at least one of the third port and the fourth port is output to the corresponding memory devices via the at least one of the first port and the second port.